In the Specification:

Page 1, before line 1, insert the following:

This application is a divisional of Application No. 09/049,626, filed March 27, 1998, now US 6,199,182, which claimed priority from Application No. 60/041,729.

Page 5, at the end of the page, insert the following:

Brief Description of the Drawings

Figure 1 is a block diagram of a known electrical circuit having three memories.

Figure 2 is a block diagram of one memory part of Figure 1.

Figure 3 is a block diagram of a circuit having a 3-bit scan path.

Figures 4A and 4B are block diagrams of a bypass memory of Figure 3.

Figure 5 is a block diagram of three circuits of Figure 3 connected in series to a tester.

Figure 6 is a block diagram of N circuits connected on a scan path in a known manner.

Figure 7 is a block diagram of N circuits connected on a scan path according to the disclosed invention.

Figure 8 is a block diagram of N circuits connected on a scan path and depicting N progressive scan test patterns.

Figure 9 is a block diagram of a circuit similar to that in Figure 3 with only a 2-bit scan path.

Figure 10 is a block diagram of a circuit similar to that in Figure 3 with a greater number of outputs than inputs.

Figure 11 is a block diagram of a scan cell C of Figure 10.

Figure 12 is a block diagram of the circuit of Figure 10 modified to accept the warping scan test concept.

Figure 13 is a block diagram of a summing cell (DSC).

Figure 14 is a block diagram of a scan testable circuit.

Figure 15 is a block diagram of a data retaining cell (DRC).

Figure 16 is a block diagram of an implementation of a warping scan test concept.

Figure 17 is a block diagram of another implementation of a warping scan test concept.

Figure 18 is a block diagram of another implementation of a warping scan test concept.

Figure 19 is a block diagram of a data capture boundary cell (DCBC).

Figure 20 is a block diagram of a data retaining boundary cell (DRBC).

Figure 21 is a block diagram of a data summing boundary cell (DSBC).

Figure 21A is a block diagram of a realization of DCBC, DRBC, and DSBC.

Figure 22 is a block diagram of circuits C1-CN being tested inside an IC or die.

Figure 23 is a block diagram of ICs 1-N being tested on a circuit board.

Figure 24 is a block diagram of boards BD being tested in a box.

Figure 25 is a block diagram of multiple boxes 1-N being tested in a system.

Figure 26 is a representation of dies being tested on a wafer.

Figure 27 is a block diagram of a test access port on a die.

Figure 28 is a representation of wafers, each carrying dies, being tested in a lot.

Figure 29 is a representation of wafer lots 1-N being tested.

Figure 30 is a block diagram of a circuit and scan path with conventional signature analyzers.

Figure 31 is a representation of a wafer with additional bussing and test pads.

Figure 32 is a block diagram of a test access port on a die.

Figure 33 is a block diagram of a conventional IEEE STD 1149.1 scan cell.

Figure 34 is a block diagram of a circuit using four conventional scan cells S.

Figure 35 is a block diagram of a circuit similar to that of Figure 34.

Figure 36 is a block diagram of a circuit relating to an input buffer.

Figure 37 is a block diagram of a circuit relating to a bi-directional pad.

Figure 38 is a block diagram of the circuits of Figures 34-37 bussed together on a die.

Figure 39A is a block diagram of a 3-state output buffer.

Figure 39B is a block diagram of a known ESD circuit.

Figure 39C is a block diagram of another known ESD circuit.

Figure 40A is a block diagram of a tester and an input buffer.

Figure 40B is a block diagram of a known ESD circuit.

Figure 41 is a block diagram of a tester and an analog output buffer.

Figure 42 is a block diagram of a tester and an analog input buffer.